Tokyo University of Agriculture and Technology

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Successful Development of World's First Vertical Ga_2O_3 Transistor through Low-Cost, Highly-Manufacturable Ion Implantation Doping Process

Researchers at the National Institute of Information and Communications Technology (NICT) and Tokyo University of Agriculture and Technology (TUAT) demonstrate a vertical Ga_2O_3 metal-oxide-semiconductor field-effect transistor (MOSFET) that adopts an all-ion-implanted process for both *n*-type and *p*-type doping, paving the way for new generations of low-cost and highly-manufacturable Ga_2O_3 power electronic devices.

Power electronics is concerned with the regulation and conversion of electric power in such applications as motor drives, electric vehicles, data centers, and the grid. Power electronic devices, namely rectifiers (diodes) and switches (transistors), form the core components of power electronic circuits. Today, power devices made of silicon (Si) are the mainstream but they are approaching fundamental performance limitations, rendering the commercial power systems bulky and inefficient. A new generation of power devices based on the wide-bandgap semiconductor – gallium oxide (Ga_2O_3) – is expected to revolutionize the power electronics industry. Ga_2O_3 promises dramatic reductions in the size, weight, cost, and energy consumption of power systems by increasing both the power density and power conversion efficiency at the device level.

The groundbreaking demonstration of the first single-crystal Ga_2O_3 transistor by NICT in 2011 galvanized intensive international research activities into the science and engineering of this new oxide semiconductor [1]. For the past several years, the development of Ga_2O_3 transistors has focused on a lateral geometry. However, lateral devices are not amenable to the high currents and high voltages required for many applications owing to large device areas and reliability issues arising from self-heating and surface instabilities. In contrast, the vertical geometry allows for higher current drives without having to enlarge the chip size, simplified thermal management, and far superior field termination. The properties of a vertical transistor switch are engineered by introducing two types of impurities (dopants) into the semiconductor – *n*-type doping, which provides mobile charge carriers (electrons) to carry electrical current when the switch is in the on-state; and *p*-type doping, which enables voltage blocking when the switch is in the off-state. A group at NICT led by Masataka Higashiwaki has pioneered the use of Si as an *n*-type dopant in Ga_2O_3 devices, but the community has long struggled to identify a suitable *p*-type dopant. Earlier this year, the same group published on the feasibility of nitrogen (N) as a *p*-type dopant [2]. Their latest accomplishment involves

integrating Si and N doping to engineer a Ga_2O_3 transistor for the first time, through a high energy dopant introduction process known as ion implantation.

"Our success is a breakthrough development that promises a transformational impact on Ga_2O_3 power device technology," said Higashiwaki, Director of the Green ICT Device Advanced Development Center at NICT. "Ion implantation is a versatile fabrication technique widely adopted in the mass production of commercial semiconductor devices such as Si and silicon carbide (SiC) MOSFETs. The demonstration of an all-ion-implanted vertical Ga_2O_3 transistor greatly enhances the prospects for Ga_2O_3-based power electronics."

This study, published December 3 in the IEEE Electron Device Letters as an early access online paper and scheduled to appear in the January 2019 issue of the journal, builds on an earlier one in which a different acceptor dopant was used [3]. "We initially investigated magnesium for *p*-type doping, but this dopant failed to deliver its expected performance since it diffuses significantly at high process temperatures," said Man Hoi Wong, a researcher of the Green ICT Device Advanced Development Center and the lead author of the paper. "Nitrogen, on the other hand, is much more thermally stable, thereby creating unique opportunities for designing and engineering a variety of high-voltage Ga_2O_3 devices."

The Ga_2O_3 base material used for fabricating the vertical MOSFET was produced by a crystal growth technique called halide vapor phase epitaxy (HVPE). Pioneered by Profs. Yoshinao Kumagai and Hisashi Murakami at TUAT, HVPE is capable of growing single-crystal Ga_2O_3 films at high speeds and with low impurity levels [4]. Three ion implantation steps were performed to form the *n*-type contacts, *n*-type channel, and *p*-type current blocking layers (CBLs) in the MOSFET (Fig. 1). The device showed decent electrical properties including an on-current density of 0.42 kA/cm^2, a specific on-resistance of 31.5 $m\Omega \cdot cm^2$, and a high drain current on/off ratio larger than eight orders of magnitude (Fig. 2). Further improvements in its performance can be readily achieved with improved gate dielectric quality and optimized doping schemes.

According to Higashiwaki and Wong, "Vertical power devices are the strongest contenders to combine currents over 100 A with voltages over 1 kV – the requirements for many medium- and high-power industrial and automotive electric power systems." The technological impact of Ga_2O_3 will be substantially bolstered by the availability of melt-grown native substrates – one of the key enablers of the silicon industry that dominates the global semiconductor market with an annual revenue of several hundred billion U.S. dollars. "The commercialization of vertical SiC and gallium nitride (GaN) power devices has, to a certain extent, been hindered by the high cost of substrates. For Ga_2O_3, the high quality and large size of native substrates offer this rapidly emerging technology a unique and significant cost advantage over the incumbent wide-bandgap SiC and GaN technologies," the researchers explained.

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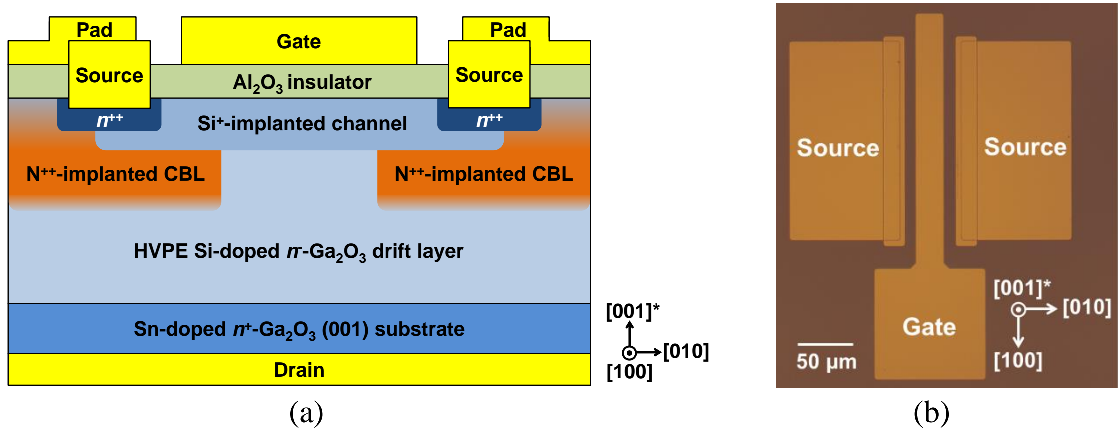

Fig. 1 (a) Cross-sectional schematic and (b) plan-view optical micrograph of the vertical Ga_2O_3 MOSFET.

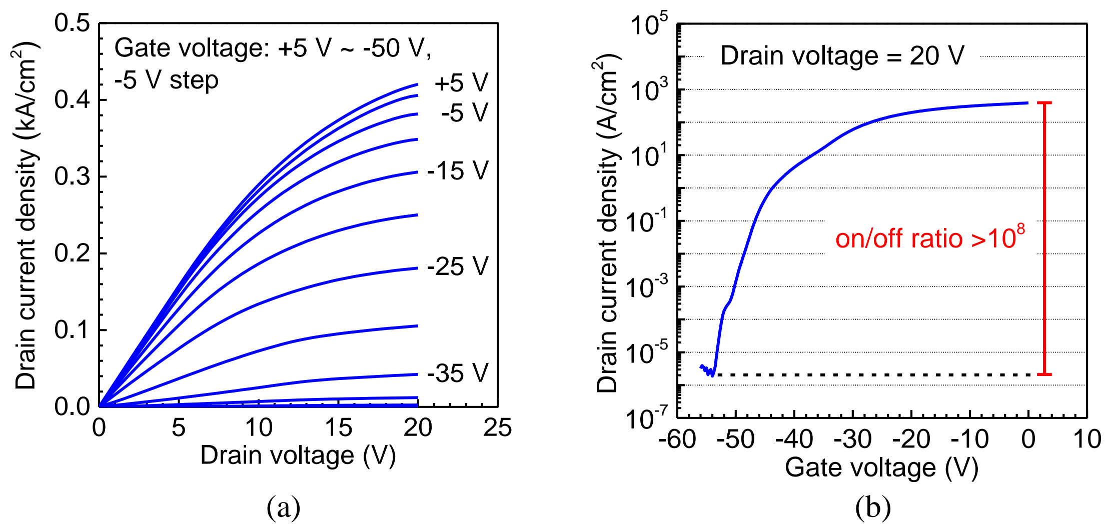

Fig. 2 (a) DC output and (b) transfer characteristics of the vertical Ga_2O_3 MOSFET.